**COS10004: Computer Systems**

**Lab 2**

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**Part 1: 4-bit adder**

Diagram

Description automatically generated

|  |  |  |
| --- | --- | --- |
| **Input A** | **Input B** | **Output** |
| 0101 | 0000 | 0101 |
| 0101 | 0001 | 0100 |
| 0101 | 0010 | 0111 |
| 0101 | 0011 | 0110 |
| 0101 | 0100 | 0011 |
| 0101 | 0101 | 0010 |
| 0101 | 0110 | 0000 |
| 0101 | 0111 | 0001 |
| 0101 | 1000 | 1101 |
| 0101 | 1001 | 1100 |
| 0101 | 1010 | 1111 |
| 0101 | 1011 | 1110 |
| 0101 | 1100 | 1011 |
| 0101 | 1101 | 1010 |
| 0101 | 1110 | 1000 |
| 0101 | 1111 | 1001 |

**Part 2: Storing bits with Flip Flops**

Diagram

Description automatically generated

|  |  |  |  |
| --- | --- | --- | --- |
| **Set** | Reset | Q | Q’ |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 |

11. When one of the inputs is 1, one of the two output LEDs is on simultaneously. This can be used for creating the circuit based on different standards.

12. After setting two inputs to 1, the two LEDs output are turned off. Based on the rules of flip flop, the output should be regarded as the complement of each of them, whereby the circuit will not accept this circumstance.

**Part 3: D Flip Flop**

Diagram

Description automatically generated

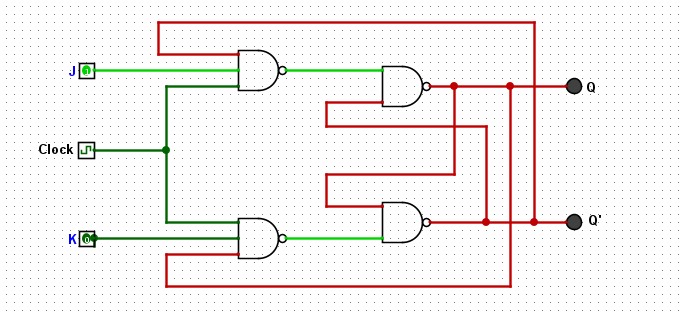
|  |  |  |  |
| --- | --- | --- | --- |
| **Clock** | **Pin** | **Q** | **Q’** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |

15. There is only 1 input in the D Flip Flop, which will have the same value with Q if the clock in the circuit goes active.

16. The clock helps evaluate and determine the signal provided in the circuit. To elaborate, when the signal determined by the clock is high, the inputs become active and the reverse situation.

17. D Flip Flop is more preferred since it does not require extra pins from designers to convert from serial to parallel like R-S Flip Flop.

**Part 4: J-K Flip Flops**



|  |  |  |  |
| --- | --- | --- | --- |
| **J** | **K** | **Q (when clocked)** | **Q’ (when clocked)** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |

20. The J-K Flip Flop will require a NOT gate to generate like the D Flip Flop

21. J and K inputs have to be both “1”